Amendments to the Specification

Kindly amend the specification as follows:

Page 1, between the title and the heading "**BACKGROUND OF THE INVENTION**", insert

--CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional application of application Serial No. 10/259,351, filed September 30, 2002, which is a divisional application of Serial No. 09/713,025 filed November 16, 2000, now U.S. Patent No. 6,495,889, which are hereby incorporated by reference in their entirety for all purposes.—

Please amend the title as follows:

A METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE ~~AND METHOD FOR MANUFACTURING SAME~~ HAVING SELF-ALIGNED CONTACTS

Please replace the paragraph beginning on page 24, line 17 with the following amended paragraph:

In this fourth example, though, in forming the silicon oxide layer 29 in the second step, the film formation material or conditions [[is or]] are set and the silicon oxide layer 29 is formed so that the space between the gate electrodes 21 in the dense region 37 will be filled in and the film thickness on the upper side 21b of the gate electrodes 21 in

the sparse region 39 will be greater than the film thickness at the side walls 21a of the gate electrodes 21 in the sparse region 39.

Please replace the paragraph beginning on page 24, line 25 with the following amended paragraph:

Specifically, in this second step, the silicon oxide layer 29 is formed after the film formation material or conditions [[is or]] are purposely selected so that the step coverage characteristics will be poor. Consequently, as shown in Figure 6(B), in the sparse region 39, for instance, the gate electrodes 21 are independent, so the silicon oxide layer 29 at the side walls 21a of the gate electrodes 21 is thinner than the silicon oxide layer 29 at the upper sides 21b of the gate electrodes 21. The silicon oxide layer 29 at the upper sides 21b of the gate electrodes 21 in the dense region 37 is substantially the same thickness as the silicon oxide layer 29 at the upper sides 21b of the gate electrodes 21 in the sparse region 39. Furthermore, since the gate electrodes 21 are densely gathered in the dense region 37, the space between the gate electrodes 21 can be filled in by the silicon oxide layer 29.

Please replace the paragraph beginning on page 25, line 14 with the following amended paragraph:

It is preferable to use PSG (phosphosilicate glass), BPSG (boron-

phosphosilicate glass), P-TEOS · NSG (non-doped silicate glass formed by plasma deposition using tetraethylorthosilicate glass), or P-SiH_4 · NSG (non-doped silicate glass formed by plasma deposition using silane), for example, as the material for forming this silicon oxide layer 29.

Please replace the paragraph beginning on page 26, line 16 with the following paragraph:

In the third step of the fourth example, however, since a specific film forming material or conditions [[is or]] are selected, as shown in Figure 6(C), the silicon oxide layer 29 is allowed to remain behind such that the film thickness at the side walls 21a of the gate electrodes 21 in the dense region 37 is greater than the film thickness at the side walls 21a of the gate electrodes 21 in the sparse region 39. Specifically, the lower side wall spacer precursor layer 29a in contact with the gate electrodes 21 in the dense region 37 is formed thicker, and the lower side wall spacer precursor layer 29a in contact with the gate electrodes 21 in the sparse region 39 is formed thinner.

Please replace the paragraph beginning on page 27, line 19 with the following amended paragraph:

Following the fifth ~~example~~ step, an interlayer insulation film 33 is formed in the sixth step shown in Figure 7(B) so as to cover the gate electrodes 21 on which the side

wall spacers are formed. This sixth step can be carried out in the same manner as the sixth step in the second example.

Please replace the paragraph beginning on page 27, line 24 with the following amended paragraph:

Following the sixth ~~example~~ step, contact holes 25 that go through the interlayer insulation film 33 are formed in self-aligning fashion by etching this interlayer insulation film 33 in the seventh step shown in Figure 7(C). This seventh step can be carried out in the same manner as the seventh step in the second example.

Please replace the abstract with the following amended abstract:

A method of manufacturing a semiconductor device ~~comprises an SAC~~ having self-aligned contact structure ~~having~~ with side wall spacers and offset nitride films. The method includes forming ~~In particular, in this semiconductor device~~[[,]] the side wall spacers ~~are constituted from~~ as having lower side wall spacers that are composed of silicon oxide films and that are in contact with [[the]] lower sides [[side]] of [[the]] gate electrode side walls, and as having upper side wall spacers that are composed of silicon nitride films and that are in contact with [[the]] upper sides [[side]] of the gate electrodes side walls. ~~As a result thereof, a~~ A distance is thus formed between the device substrate and [[the]] an interface between the silicon nitride film and the silicon

oxide film. This suppresses the hot carrier phenomenon and the occurrence of poor contact.